Symmetry Breaking of Electronic States in Graphene Manifested Through Electrical Transport in High Magnetic Field

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Introduction

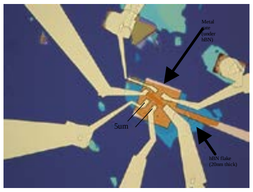
The focus of our work on graphene is correlated electron phases that arise at low temperatures and in high magnetic fields. To access these intrinsic properties we investigate the influence of the substrate on graphene. We suspend graphene over the substrate (SG) [1], employ high quality substrates such as hexagonal boron nitride (GBN)[2] or combine these methods.

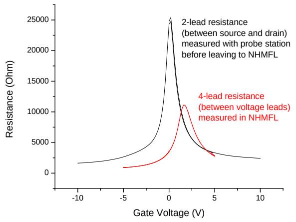
Experimental

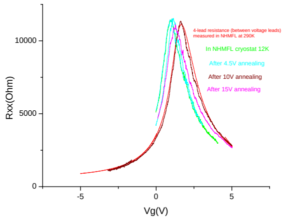
The fabrication of SG and GBN devices is described in [1] and [2] respectively. A combination of these methods was used to make hybrid devices. During our visit to NHMFL we used 31T magnet in cell 9 with ^{3}He cryostat. For measurement of electric transport we employed dual Keithley 6221, 2182a Delta mode setup [3].

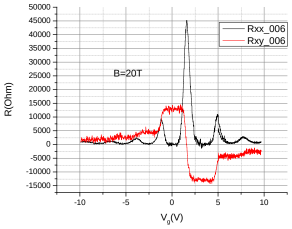
Results and Discussion

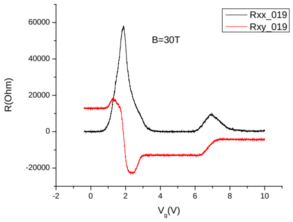
In attempt to screen traps in SiO_2 substrate we fabricated a device with **metallic gate under hBN substrate**. The figure below shows (from left to right): optical image; R_{xx} vs V_{gate} for B=0 after transporting device to NHMFL; effect of current annealing; magnetotransport in 20T; and in 30T. This device, unlike suspended graphene devices, had very weak and inconsistent response to current annealing. A possible explanation is that metal gate (gold) under thin hBN substrate dissipates heat so efficiently, that the temperature of graphene never rises significantly above the temperature of the environment. Due to being unable to improve the sample quality, we also could not observe sought-after effects of symmetry-breaking and interactions, insulating state and FQHE. While the device did display a sequence of plateaus characteristic of IQHE in single layer graphene, these were the only features, and Rxx never reached high values despite us trying as low an excitation current as the noise environment would allow (1nA) and working in temperatures of a few Kelvin.











Suspended graphene device: Despite the success of current annealing for our SG device (residual carrier density due to puddles is $1.5x10^9 cm^{-2}$, mobility as high as 320000 $cm^2V^{-1}s^{-1}$, mean free path over 200nm), we did not observe any features of QHE in this device.

Conclusions

1. The device quality deteriorates after transportation. 2**.** Only devices which are not in contact with a substrate (on either side of graphene) can be improved by current annealing. 3**.** Using metallic gate by itself does not solve the problems associated with charge traps.

Acknowledgements

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References

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[2] Dean, C. R. *et al*. Nature Nanotechnology **5**, 722–726 (2010).
[3] A. Suslov, NHMFL, Private communications