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The continuous demand on miniaturized electronic circuits bearing high power density illuminates the need to modify the silicon-on-insulator-based chip architecture. This is because of the low thermal conductivity of the few hundred nanometer-thick insulator present between the silicon substrate and active layers. The thick insulator is notorious for releasing the heat generated from the active layers during the operation of devices, leading to degradation in their performance and thus reducing their lifetime. To avoid the heat accumulation, we propose a method to fabricate the silicon-on-diamond (SOD) microstructure featured by an exceptionally thin silicon oxycarbide interlayer (∼3 nm). While exploiting the diamond as an insulator, we employ spark plasma sintering to render the silicon directly fused to the diamond. Notably, this process can manufacture the SOD microarchitecture via a simple/rapid way and incorporates the ultra-thin interlayer for minute thermal resistance. The method invented herein expects to minimize the thermal interfacial resistance of the devices and is thus deemed as a breakthrough appealing to the current chip industry. *Published by AIP Publishing.* https://doi.org/10.1063/1.5030580

In the recent silicon-on-insulator (SOI) technology, diamond serves as an insulator, which is alternative to the conventional SiO_2, since diamond provides outstanding thermal conductivity and appreciable electrical insulation.[1–4] The diamond layer-inserted silicon-on-diamond (SOD) microarchitecture thus shows potential in further enhancing the operating performance by efficiently dissipating the heat from the devices.[5–7] Most SOD studies in the past few decades focused on growing the diamond layer on silicon wafers through chemical vapor deposition (CVD), after which the diamond is polished to include a smooth surface, ideally used to deposit active layers.[8] This strategy, however, leaves the diamond surface rough even after post-polishing and therefore presents difficulties in stacking active layers onto the diamond via rigid bonding. Therefore, the insertion of a SiO_2 film with a thickness of hundreds of nanometers above the diamond layer is mandatory in this fabrication method to achieve phenomenal adhesion among all layers inherent to the SOD microarchitecture.[9] The thick SiO_2 interlayer combined with its low thermal conductivity, again, hampers the dissemination of heat produced during the operation, thereby frequently declining the device performance. Several attempts have been performed to exclude the SiO_2 interlayer from the SOD architecture such as pulsed laser-driven, plasma-activated, or ultra-high vacuum-assisted thermal energy-bonding techniques.[10–13] Among these methods, the microwave plasma-CVD deposition method is successful in reducing the interlayer thickness present in the GaN-on-diamond (GOD) architecture, where silicon innate to the SOD structure is replaced by GaN: The thickness of the dielectric SiN interlayer for the GOD architecture is decreased to show 30 nm.[14] Yet, the interlayer thickness is not thin enough to provide the resulting device with negligible thermal resistance.

To assert that the SOD structure is indeed viable to build the device exempting from the heat management issue, one must amend the SOD to not contain a thick thermal resistor between the active layer and the diamond. Several articles have reported that diamond is physically robust and chemically inert; therefore, it is incompatible with other materials.[15] The physicochemically sturdy diamond seems not to be metallurgically engineered but can seek compromise to fuse with silicon via the spark plasma sintering (SPS) process. The SPS process is reported to employ the Joule heating principle for efficiently consolidating powder, joining, or welding non-compatible materials at lower temperatures (1000 °C) within shorter operating times (∼2 min) than those of the conventional hot pressing bonding process (≥1100 °C for 22 h).[16–18] [Fig. 1(a)] We performed a series of control experiments to locate the appropriate temperature (T_{SPS}) required to construct a stable *micro*-structure while minimizing any significant structural collapse of Si substrates via melting. These process parameters provide an optimum temperature range of $950\,^{\circ}C < T_{SPS} < 1100\,^{\circ}C$. This is because of the absence of any chemical fusion on interlayers at ≤950 °C and the complete digestion of Si substrates at ≥1100 °C. These process

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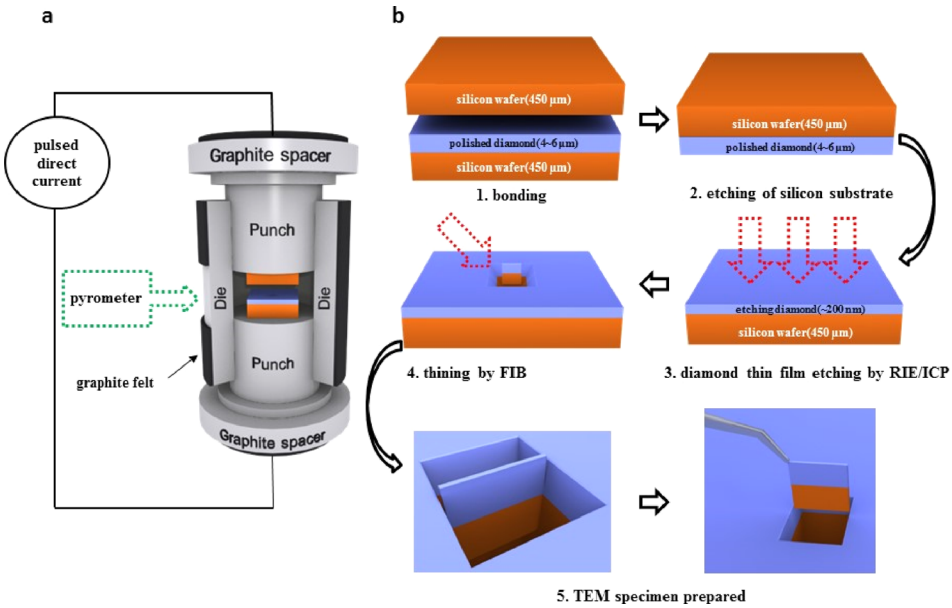

FIG. 1. (a) Schematic illustration of the spark plasma sintering (SPS) process with die assembly. (b) Transmission electron microscopy (TEM) specimen preparation involving dry etching and focused ion beam (FIB).

parameters also give an important clue about the interfacial temperature range between Si and diamond during the SPS process, which is between 1000 °C and 1100 °C. Again, this is because the resulting *micro*-structure does not reveal any considerable damage on Si substrates, which is only obtainable if the interfacial temperature is <1100 °C.

The promise provided using the SPS process to construct the SOD architecture is also supported by our previous study, which attempts to produce the GOD microstructure.[19] It is noteworthy that the ideal GOD architecture remains challenging to evolve due to the thermodynamic limitation of Ga fusing with the diamond to form Ga carbide (i.e., Ga_4C_3) under the SPS condition employed (i.e., ~1000 °C under vacuum). This is in contrast to the SPS-derived SOD architecture because the silicon (active layer) can spontaneously fuse with diamond to produce Si carbide (SiC) or Si oxycarbide (SiCO), as evidenced by their negative Gibbs free energies under the identical SPS condition.[20,21]

Motivated by the spontaneous formation of SiC or SiCO in addition to the benefits of the SPS process, our goal in this study is to utilize the SPS process as a means to chemically fuse the dissimilar materials (i.e., diamond and silicon) to manufacture the SOD micro-architecture in a facile and fast manner. This study demonstrates that the SPS process enables the fabrication of the SOD microstructure to be highly desired and qualified while providing a void-free SiCO interlayer with a thickness of ≤ 3 nm.

The SOD microstructure is manufactured according to the experimental procedure detailed in the following paragraphs and Fig. 1(b).[22] For the microscopic observation of the interfacial region in the resulting SOD architecture, we use transmission electron microscopy (TEM). We first evaluated the integrity of the diamond-Si bond using a TEM specimen carefully obtained from the bulk SOD architecture using focused ion beam (FIB), as shown in Fig. 1(b).[22] The bonded interface is neat and flat and exhibits excellent integrity while missing any voids or weakly bonded regions [Fig. 2(a)]. More importantly, this interface shows a thickness of 2.4 ($\pm$ 0.2) nm between the diamond and the silicon. This is significantly thinner than that reported to date, as substantiated by Figs. 2(b) and 2(c). This highly suggests that our SOD architecture can release the heat efficiently from the device, which is primarily mediated by the "thin" interface with potentially negligible thermal resistance.[5]

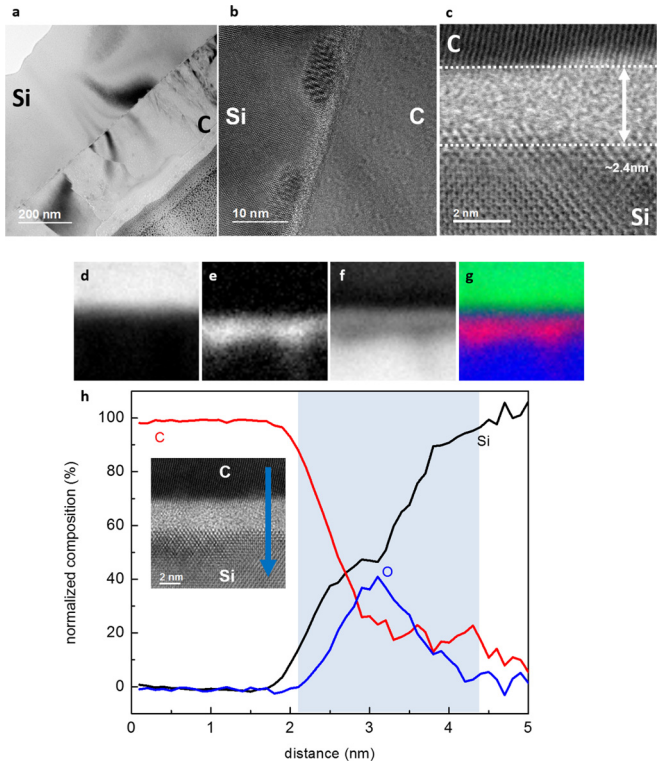

FIG. 2. Transmission electron microscopy (TEM) images of the specimen obtained via the procedure illustrated in Fig. 1(b). (a) Low-magnification bright-field TEM image of the interface. (b) High-resolution TEM image of the interface. (c) High-resolution annual bright field scanning TEM (ABF-STEM) images of the interface. Elemental maps of the interface region: (d) carbon, (e) oxygen, (f) silicon, and (g) total composition map, where green is carbon, red is oxygen, and blue is silicon. (h) Composition profiles across the interface collected from the diamond side (distance of 0 nm) to the silicon side (distance of 5 nm). (Note: The blue-shaded rectangle indicates the interface regime.)

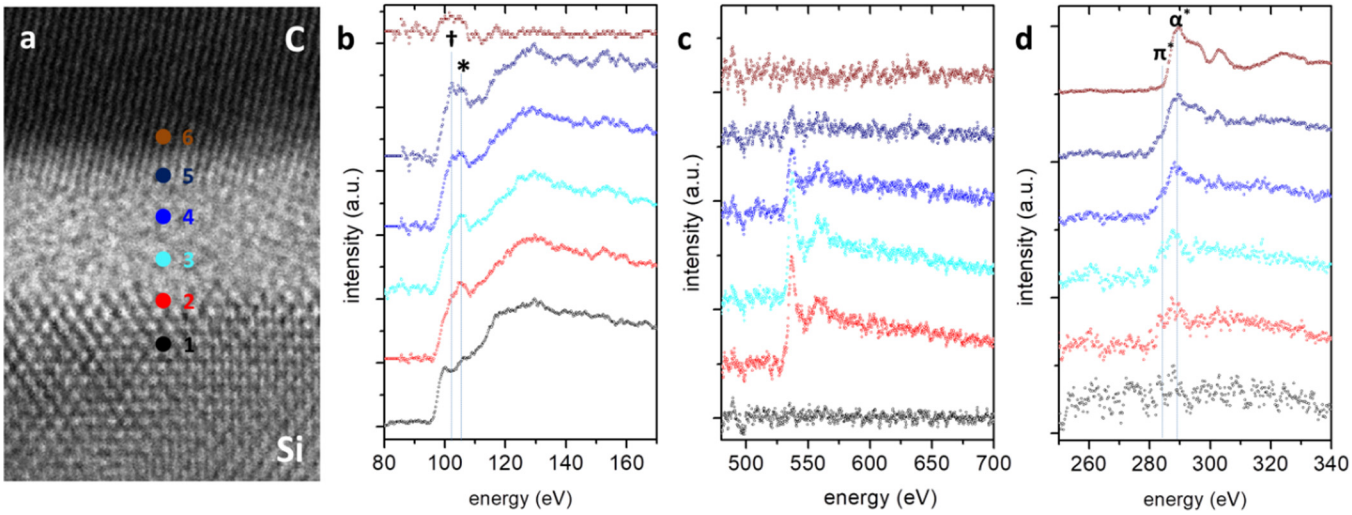

FIG. 3. Electron energy loss spectroscopy (EELS) spectra across the interlayer. (a) ABF-STEM image including spots with different colors, where EELS spectra are observed and illustrated herein (Note: black for 1, red for 2, cyan for 3, blue for 4, navy for 5, and wine for 6). (b) Si $L_{2,3}$-edge. (Note: † and * denote the features for SiC and SiO_2, respectively.). (c) O K-edge. (d) C K-edge. (Note: π^* and α^* indicate the features for the sp^2-hybridized and sp^3-hybridized C-C bonds, respectively.)

We also used electron energy loss spectroscopy (EELS) in the scanning TEM mode (STEM-EELS) for the elaboration of the chemical composition and structural information inherent to the thin interface. The interface primarily consists of silicon, oxygen, and carbon, as clarified in the elemental maps in Figs. 2(d)–2(h). The composition profiles across the interface show that the oxygen content is the highest in the middle of the layer, whereas the carbon content is the highest at the diamond side and gradually decreases towards the silicon side, which is counter-current to the trend for silicon.

To further examine the nature of bonds inherent to the interlayer, its electron energy loss near edge structure (ELNES) for Si, C, and O species was also inspected. When traversing the interlayer from the silicon side to the diamond side (i.e., ***1*** → ***6*** in Fig. 3), the spectra in the Si-$L_{2,3}$ edge show a shift in the major peak location under the onset edge from 106 eV (* in ***2*** and ***3***) to 102 eV († in ***4*** and ***5***), each of which exhibits the character for SiO_2 and SiCO, respectively.[23,24] The interlayer spectra in the O-K edge show a single, sharp peak at ∼535 eV (i.e., ***2–5***), resulting from the O-O scattering feature.[25] The sharp peak of the O core loss arises from the O-O scattering, and its intensity decrease means that the number of oxygen in the second nearest neighbors is reduced. This indicates that more Si-O bonding exists in the middle of the layer. At the same location, the increase in C is due to the increased C core loss peak height. All three Si, O, and C spectra indicate the SiCO compound. Interlayer spectra in the C-K edge consistently show the σ^* peak at ∼290 eV, resulting from the sp^3-hybridized C-C bond,[26] whereas the π^* peak assigned as the sp^2-hybridized C-C bond is also observed at ∼285 eV.[27] This suggests that the interlayer is amorphous, which is also in close agreement with the ABF-STEM image of the interlayer showing indiscernible lattice fringes [Fig. 2(c)].

To conclude, we postulate that 1–2 nm-thick, passivated silicon (SiO_{2-X}) is present on the silicon layer even after cleaning, and therefore, it participates indispensably in fusing with diamond to generate the SiCO interlayer in the resulting SOD architecture. We also conjecture that a high temperature generated under the SPS condition creates a molten zone between the diamond and the silicon layers, wherein the carbon in diamond and the SiO_{2-X} in the silicon undergo dynamic thermal diffusion to form the SiCO interlayer.[28] The SiCO interlayer undoubtedly provides a lower thermal conductivity (∼0.1 W m^{-1} K^{-1}) than SiO_2 (∼1 W m^{-1} K^{-1}).[29] Our fabrication method, however, is capable of creating an "exceptionally" thin interlayer between the diamond layer and the active silicon layer. The ultrathin SiCO interlayer is thought to compensate for or even surpass the conventional thick interlayers with greater thermal conductivities for achieving negligible thermal resistance during the device operation (Fig. 4).[30,31] The fabrication of electronic devices through the deposition of active layers onto our SOD structure and its long-term performance comparison with other conventional analogues are currently performed in our research lab.

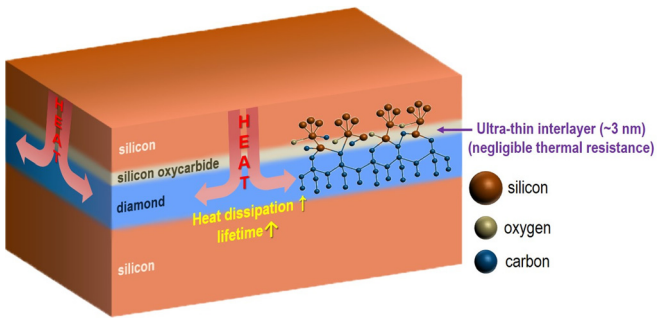

FIG. 4. Schematic of the fabricated silicon-on-diamond (SOD) architecture.

See supplementary material for experimental methods and characterization conditions of TEM and EELS.

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